Karim Sabra

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Summary

Final-year Master's student in Microelectronics Engineering and Semiconductor Physics (Diplôme d'ingénieur) with hands-on experience in digital and analog IC design and verification. Graduating in September 2026 and open to relocation; actively seeking opportunities in digital design, hardware verification, mixed-signal IC development, or neuromorphic computing.

Experience

CNRS **Lyon, France**
Apprentice Engineer – Mixed-Signal ASIC Design/Verification *Sep 2023 – Present (2 years)*

- Designed and verified a tri-axial particle detector front-end integrating both digital and analog circuitry.
- Developed a Phase-Locked Loop (PLL) subsystem from concept to tape-out, including PFD, charge pump, VCO, frequency divider, and digital control; created behavioral models and integrated the PLL into the overall system.
- Performed post-layout verification with extracted parasitics, conducting jitter analysis and lock-time measurements to drive layout refinements.

Microelectronics Institute of Seville **Seville, Spain**
Mixed-Signal Verification Intern *July 2025 – Sept 2025 (3 months)*

- Verified and simulated sigma-delta ADC modulators to support an AI-driven analog design automation flow.
- Developed an automated simulation pipeline using Cadence OCEAN and Python to run 200+ test cases with parameter sweeps and logged results, including scripted validation checks.
- Created a Python-based GUI tool to configure simulation parameters and orchestrate Cadence Spectre/OCEAN runs, enabling efficient dataset generation for machine learning (ML).

Selected Projects

RTL and SoC Design Projects – CPE Lyon 2024 – 2025 (1 year)

- Integrated open-source processor cores (RISC-V and NEO430) with custom on-chip peripherals ; developed comprehensive VHDL testbenches to verify system functionality.
- Designed small DSP IP blocks and implemented a UART transmitter/receiver with finite state machines (FSMs) and a baud-rate generator for serial communication.

X-HEEP + Vicuna integration, FPGA prototype 2025 — *in progress*

- Studying X-HEEP architecture, memory banks, bus interfaces, and CLINT/PLIC interrupts.
- Reviewing Vicuna's coprocessor interface and supported RISC-V V instructions.
- Defining the integration path via X-HEEP's exposed master/slave ports and the core-v-x interface on cv32e40x.
- Building a simulation harness with smoke tests for vector ops (add, multiply, AXPY).

Education

CPE Lyon (Graduate School of Engineering) Lyon, France

- Master's in Microelectronics Engineering and Semiconductor Physics (Diplôme d'ingénieur) *Expected Sep 2026*
- Bachelor's in Microelectronics and Semiconductor Physics *Graduated 2024*

Skills

- Digital design: RTL design, microarchitecture, Verilog, VHDL, SystemVerilog, control finite state machines (FSMs), SoC integration, UVM (training in progress)
- EDA tools: Cadence Virtuoso, Spectre/Spectre-X, OCEAN, Cadence Maestro, Xilinx Vivado, Git, Linux
- Analog/mixed-signal: Mixed signal design and verification, Analog and digital layout , post-layout verification.
- Programming: Python, C, MATLAB, Bash
- Languages: French (native), English (fluent), Arabic (fluent)