Karim Sabra

Lyon, France | +33 6 68 85 09 44 | karimsabra926@gmail.com
linkedin.com/in/karim-sabra-633007235 | karimsabra.com

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Summary

Final-year microelectronics engineering student (Master's), graduating Sep 2026. Focus on digital design and verification for SoC and FPGA. RTL, SystemVerilog/UVM, SVA, coverage. Strong automation with Python and OCEAN. Mixed-signal context from PLL and TDC work applied during apprenticeship and research internship. Target roles: digital and mixed design, verification, RISC-V, AI-assisted EDA. Willing to relocate. References available on request

Skills

- **Digital design**: **RTL**, microarchitecture, **SoC**, RISC-V, FSMs, **Verilog, SystemVerilog**, Verilator, FPGA (Vivado)
- **Verification**: **UVM**, SVA, constrained random, coverage, **Xcelium**, cocotb, assertions, STA, Verilator
- **Analog/mixed-signal**: Virtuoso, Spectre, OCEAN, PLL, TDC, ADC/DAC, post-layout checks
- **Software**: **Python**, C, Assembly, Shell, MATLAB, Git, Linux, Zephyr
- **Languages**: French, English, Arabic

Experience

CNRS, Institut de Physique des 2 Infinis (IP2I) — **Lyon, France**
Apprentice Engineer, Mixed-Signal ASIC — *Sep 2023 - Present (3 years)*

- Mixed-signal **design and verification** for a PLL on PICMIC-1 from behavioral to transistor level
- Detailed DC, transient, stability, and AC simulations on the PLL.
- Migration note from TSMC 130 nm to TowerJazz 180 nm with consistent phase-noise profile. Post-layout checks with extracted parasitics
- Key numbers: 1.5 to 2 us lock time. Jitter 2 ps rms pre layout and 7 ps rms post layout at 2.58 GHz

IMSE-CNM (CSIC/US) — **Seville, Spain**
Research Intern, Mixed-Signal Verification — *Jul 2025 - Sep 2025 (3 months)*

- **Verification and dataset generation** for CT sigma-delta modulators across Active-RC and Gm-C variants
- Unified **OCEAN** automation and a Python GUI to configure 200+ parameterized Spectre runs with pass or fail checks enabling rapid regression for ML dataset generation
- KPIs: SNR, SNDR, ENOB, bandwidth. CSV exports and plotting templates for fast comparison

Projects

HOLYCORE, RV32I single-cycle core — **Side project**, 2025

- **RTL** for RV32I from scratch , clean datapath and control, ALU, byte-enable memory, typed opcodes and ALU enums
- **Verification**, cocotb unit and top tests, randomized ALU checks, scoreboarding, ISA smoke programs on Verilator, coverage targets for arithmetic, control flow, and memory classes
- Integration readiness, simple memory map, reset and exception stubs, build scripts and waveform presets

Heterogeneous smart parking, Edge AI + FPGA + MCU — **CPE Lyon**, 2025

- **FPGA control path**, Nexys A7 with **VexRiscv (RV32IM)** with linux
- Verilog FSM driving the barrier, Ethernet communication, telemetry, and latency counters
- Vision chain on BeagleY-AI, IMX219 camera, AI **TIDL** models on DSP
- Focus on **systems integration**, clear interfaces between inference and RTL actuation
- Group project, managing the coordination of different parts of the project to ensure compatibility across all team contributions.

Education

CPE Lyon, Graduate School of Engineering — Lyon, France

- Master's in Microelectronics Engineering and Semiconductor Physics *(Engineering Diploma)* — *Expected Sep 2026*
- Bachelor in Microelectronics and Semiconductor Physics — *2024* (Ranked 2nd in the class)